Software

Matrox **FPGA Developer's Toolkit (FDK)**

Altera® edition

Development toolkit for custom FPGA-based image processing.

Key features

- quickly create custom FPGA configurations for Matrox image processing hardware based on Altera® devices
- graphically design FPGA configurations using Altera®'s SOPC Builder tool
- assemble FPGA configurations using a Matrox library of ready-made highly-optimized SOPC design components
- develop custom design components in VHDL
- includes Matrox productivity enhancing tools to assist in generating FPGA configurations and facilitate the creation of custom design components
- Matrox tools to test and troubleshoot FPGA configurations without writing a single line of code
- supports Microsoft® Windows® XP
- optionally bundled with Altera® Quartus® II 6.0[1,2,3]
- free first-year enrollment in maintenance and support program

Harness the full power and flexibility of FPGAs for image processing

The Matrox FPGA Developer's Toolkit (FDK) – Altera® edition is a comprehensive development suite that includes the tools and libraries necessary to quickly develop and deploy fully-customized FPGA configurations for Altera® -based Matrox image processing hardware. The Matrox FDK enables the creation of FPGA configurations that maximize the offload or acceleration of image processing functions.

Quick assembly using ready-made design components

Drag-and-drop Matrox library components within the Altera® SOPC Builder tool to easily create custom FPGA configurations. Available design components consist of carefully crafted transfers units and processing units. Design components are efficiently interconnected through the Altera® Avalon® switch fabric, which is generated by Altera® SOPC Builder. Overall integration is further simplified by way of the Matrox Constraints Generator tool, which effortlessly handles the details of arranging the FPGA configuration to work with Matrox image processing hardware. No other suite simplifies FPGA development for image processing like the Matrox FDK.

Focused development of custom image processing functions

The Matrox FDK also provides the underlying framework to simplify and facilitate the development of custom processing units for Matrox image processing hardware. This framework includes the Matrox Processing Unit Designer, the same tool Matrox designers use to generate the necessary structure around custom VHDL code to seamlessly interface with both the Matrox SOPC library and the Matrox Imaging Library (MIL). Creating custom processing units with the Matrox FDK allows developers to focus on the implementation of the core algorithms vital to the application rather than the peripheral logic.

MATROX
IMAGING

FDK productivity tools:

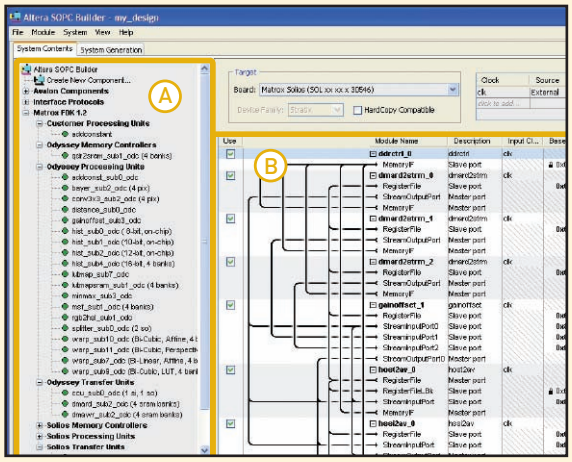
Altera® Quartus® II 6.0[3,5] (optional) including SOPC Builder

Development environment used to develop and compile FPGA configurations. Altera® SOPC Builder is an intuitive graphical interface for integrating design components into an FPGA configuration with no VHDL development required.

Matrox Processing Unit Designer

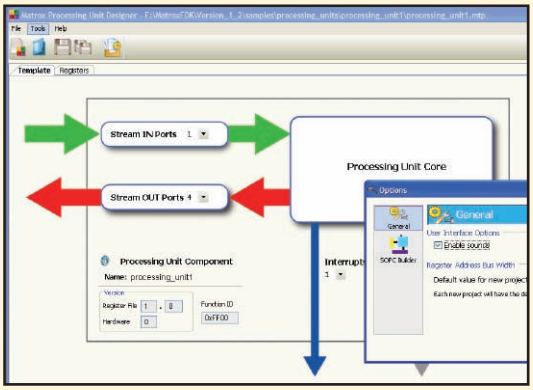
Efficiently integrates custom VHDL code with the necessary template in order to develop a custom FPGA processing unit. Integrated processing units are available for use with Matrox image processing hardware and are controlled from a software application using FPGA-specific API functions.

Altera® SOPC Builder



(A) List of available Altera®, Matrox, third-party and custom design components (B) Graphically interconnected system

Matrox Processing Unit Designer

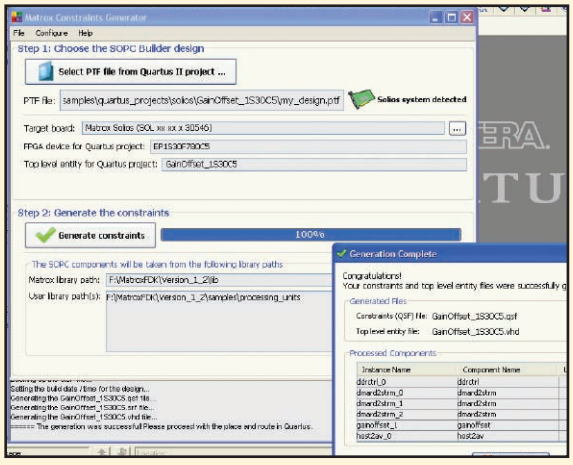


Configure the template for a custom processing unit

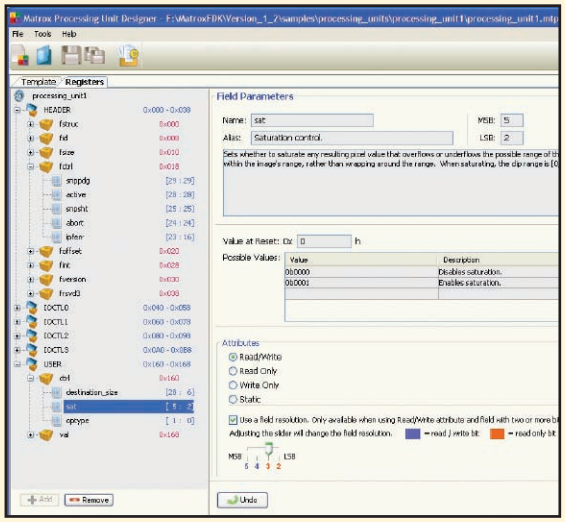
Matrox Constraints Generator

Interactive utility that automates the creation of the necessary glue logic, pin-outs and timing constraints in order to target FPGA configurations for Matrox image processing hardware.

Matrox Constraints Generator utility



Matrox Processing Unit Designer (cont.)

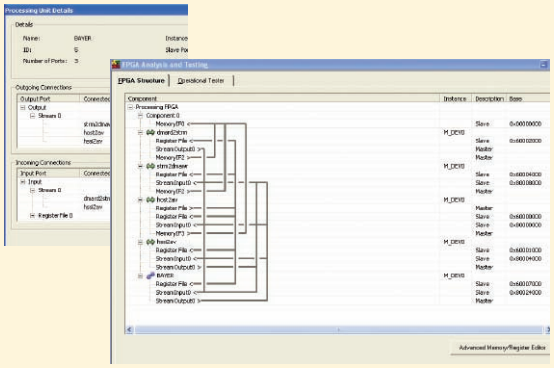


Quickly view and edit register fields for a custom processing unit

Matrox FPGA Assistant

Graphically facilitates the testing and debugging of FPGA configurations without the need to develop any software application. Capture, processing, register access and interrupt monitoring all available within this tool.

FPGA Assistant utility



Matrox library of SOPC design components[4]:

Processing Units:

Add a Constant

- add a constant value with optional saturation
- supports up to 8 bits per pixel (signed or unsigned)
- processes 8 pixels per clock cycle

Bayer Filter

- decode the color information of a single-band, Bayer color-encoded image using bilinear interpolation with optional white balancing and overflow saturation
- RGB or BGR output
- supports up to 16 bits per pixel (unsigned)
- processes up to 4 pixels per clock cycle

Convolution 3 x 3

- 3x3 convolution (FIR Filter) or grayscale erosion/dilation
- optional right shift, clipping, absolute value and selectable overscan mode
- supports up to 16 bits per pixel (signed or unsigned)
- processes up to 4 pixels per clock cycle

Distance

- determines the shortest distance from each non-zero pixel to a zero pixel
- choice of chamfer 3-4, chessboard or city block methods
- supports up to 16 bits per pixel (unsigned)
- processes 4 pixels per clock cycle

Gain and Offset

- performs a per-pixel gain and offset correction with shift and overflow saturation
- supports up to 16 bits per pixel (unsigned)
- processes up to 8 pixels per clock cycle

Histogram

- calculates the histogram (pixel intensity distribution) of the source image
- supports up to 16 bits per pixel (unsigned)
- processes up to 8 pixels per clock cycle

LUT Map

- maps each pixel in the specified source image to the values determined by the specified lookup table
- supports up to 16 bits per pixel (unsigned, mono)
- supports up to 32 bits per pixel (unsigned, packed)
- processes up to 8 pixels per clock cycle

Min and Max

- finds the minimum and maximum pixel value of an image
- supports up to 32 bits per pixel (signed or unsigned)
- processes up to 8 pixels per clock cycle

Plane Separator

- Separates a packed color image into multiple monochrome component images with optional component discard
- supports input up to 64 bits per pixel (unsigned, packed)
- supports output up to 4 channels and up to 16 bits per pixel (signed or unsigned)
- outputs up to 8 pixels per clock cycle

RGB to HSL color Space Converter

- color space conversion from RGB to HSL colour space
- supports up to 64 bits per pixel (unsigned)
- outputs up to 2 pixels per clock cycle

Splitter

- 2 or 4 way splitter produces multiple copies of the input data
- enables parallelism in the FPGA
- supports up to 64 bits per pixel (signed or unsigned)

Warping

- 3x3 matrix-defined or LUT-driven warping operation
- choice of interpolation modes (nearest-neighbor, bilinear or bicubic)
- supports up to 16 bits per pixel (signed or unsigned) and up to 32 bits per pixel for nearest-neighbor only
- processes up to 4 pixels per clock cycle

Transfer Units and Memory Controllers:

DDR SDRAM Memory controller

- interface processing FPGA to external DDR SDRAM memory for processing units[3] (for Matrox Solios family)

QDRII SRAM Memory controller

- interface processing FPGA to external QDRII SRAM Memory for processing units

High Speed Serial Interface (HSSI)

- link to the acquisition portion of the Matrox Solios

DMA Controllers

- DMA engine for reading or writing data from the memory controller(s) on the FPGA

PCI-X interface

- used to interface the switch fabric to the host bus

Supported environment

- Microsoft® Windows® XP

Additional requirements (sold separately)

If targeting Matrox Solios family:
- Matrox Imaging Library (MIL) or MIL-Lite
- Matrox Solios frame grabber with FPGA-based processing core

If targeting Matrox Odyssey Xpro+:
- Matrox Odyssey DTK
- Matrox Odyssey Xpro+

Altera® Quartus® II (if not purchased with Matrox FDK)
- Version 6.0[3] with license for Altera® DDR SDRAM controller (for Matrox Solios family only)
- Version 7.1[3] (for Matrox Odyssey Xpro+ only)

Ordering Information

Development Toolkits

Part number	Description
SOL FDK	Matrox FPGA Developer's Toolkit (FDK) for Matrox Solios. Includes CD with Matrox component library, Matrox Constraints Generator and Matrox Processing Unit Designer, FDK User Guide and a one year maintenance contract for a single developer seat. Requires Altera® Quartus® II 6.0[1,3] with DDR SDRAM and NIOS® II licenses[2]. Also requires MIL/MIL-Lite. Supports Windows® XP.
SOL FDK F	Same as SOL FDK for a single floating developer seat.
SOL FDK AQ2	Same as SOL FDK bundled with Matrox edition of Altera® Quartus® II 6.0[1,3] for Windows® XP.
ODY FDK	Matrox FPGA Developer's Toolkit (FDK) for Matrox Odyssey Xpro+. Includes CD with Matrox component library, Matrox Constraints Generator and Matrox Processing Unit Designer, FDK User Guide and a one year maintenance contract. Requires Altera® Quartus® II 7.1[1,3] with NIOS® II license. Also requires Odyssey DTK. Supports Windows® XP.

Development Toolkits (continued)

Part number	Description
ODY FDK F	Same as ODY FDK for a single floating developer seat.
ODY FDK AQ2	Same as ODY FDK bundled with Matrox edition of Altera® Quartus® II 6.0[1,3,5] for Windows® XP.

FFDK Maintenance Program

The Matrox FDK provides registered users automatic enrollment in the maintenance program for one year. This maintenance program entitles registered users to one year of technical support and free updates of the development toolkit excluding the Altera® Quartus® II 6.0 components.

Part number	Description
SOL FDK MAINT	One year maintenance contract extension.
ODY FDK MAINT	One year maintenance contract extension.

Note: Altera® Quartus® II subscriptions are renewed separately and directly with Altera® (www.altera.com)

Comprehensive yet highly accessible documentation

Online help provides users with thorough yet easy-to-find documentation covering all aspects of the Matrox FDK and the Matrox Imaging developers' forum provides direct access to a global community of other Matrox developers.

Matrox FDK Training

Accelerate development by visiting Matrox Imaging's website (http://www.matrox.com/imaging/training/) to access comprehensive self-paced video training and for more information on Matrox FDK and MIL instructor-led training courses.

Notes:

1. Does not include ModelSim® - Altera® Edition.
2. If optional Altera® Quartus® II package is not selected, this item must be purchased directly from Altera®.
3. Other versions of Altera® Quartus® II are supported, please contact your local representative or Matrox Imaging Sales for latest availability.
4. Not all library components are available for all Matrox Imaging hardware platforms. Please contact local representative or Matrox Imaging Sales for latest availability.
5. Altera® Quartus® II version 7.1 upgrade available directly from Altera®.

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